

### **Remarks**

Claims 39-41 and 57-59 were pending. Claims 71-74 have been added.

Claims 39 and 58 are independent claims. Claims 40, 41, 71, and 72 depend from independent claim 39 and claims 58, 59, 73, and 74 depend from independent claim 57.

The Examiner has indicated that claims 41 and 59 would be allowable if rewritten in independent form.

The Examiner has rejected claims 39, 40, 57, and 58 under 35 U.S.C. § 102(e) over the first embodiment of Kimura (U.S. 2002/0192901).

Each of independent claims 39 and 57 requires a first metal level disposed over the ferroelectric device level, an inter-level dielectric level disposed over the first metal level, and a second metal level disposed over the inter-level dielectric level. As shown in FIGS. 1 and 16, in the first embodiment of Kimura there is only one metal level 24 disposed over the ferroelectric device level (consisting of layers 19, 20, 21, 22). Kimura fails to teach or suggest disposing an inter-level dielectric level over metal level 24, much less disposing an inter-level dielectric level over metal level 24 and disposing an additional metal level over the inter-level dielectric level. Indeed, disposing an inter-level dielectric level over metal level 24 and disposing an additional metal level over the inter-level dielectric level would not serve any apparent useful purpose since all of the device structures in Kimura's memory device are connected to one of the three metal levels (namely, the first metal level consisting of layers 9 and 10, the second metal level consisting of layers 11 and 12, and the third metal level 24) that are already present in the device.

For at least these reasons, the Examiner's rejection of independent claims 39 and 57 under 35 U.S.C. § 102(e) over Kimura now should be withdrawn.

Claims 40, 71, and 72 incorporate the features of independent claim 39 and claims 58, 73, and 74 incorporate the features of independent claim 57. Therefore, claims 40, 71, 72, 58, 73, and 74 are patentable for at least the same reasons explained above. Claims 71-74 also are patentable for the following additional reasons.

Each of claims 71 and 73 recites that between the ferroelectric device level and the transistor isolation layer is free of any interposing metal level. As shown in FIG. 1, the first embodiment of Kimura includes a first metal level (consisting of layers 9 and 10) and a second metal level (consisting of layers 11 and 12), both of which are interposed between a

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ferroelectric device level (consisting of layers 19, 20, 21, 22) a transistor isolation layer 8.

For at least this additional reason, claims 71 and 73 are patentable over Kimura.

Each of claims 72 and 74 recites that throughout the ferroelectric isolation layer each ferroelectric isolation layer via is laterally sized larger than the corresponding contact via. Kimura does not teach or suggest such a feature. For at least this additional reason, claims 72 and 74 are patentable over Kimura.

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 50-1078.

Respectfully submitted,

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